FOSS LSI design method
for democratization of LSI fabrication without NDA

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Agenda

- Motivation: “Make: “ movement for LSI!
- Fabrication cost deduction effort in Japan
- “MakeLSI:” project outcomes (chips)
- Our design flow with Alliance

- Slides from Prof.Akita who starts “MakeLSI:”

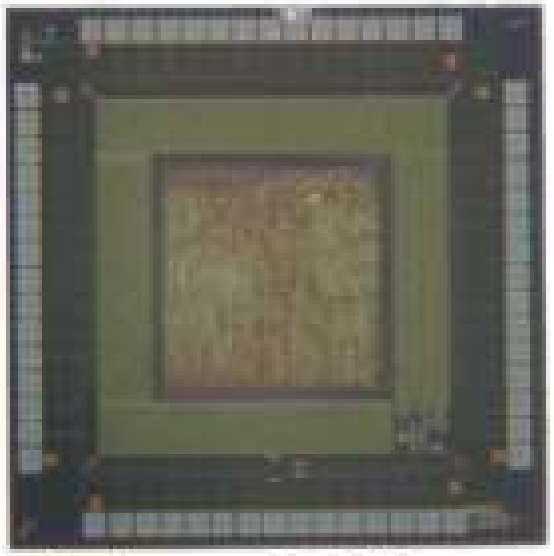
Maker Faire Tokyo 2016

- There are strong demands to make something in all generations!
- 400 exhibitors 18000 participants!

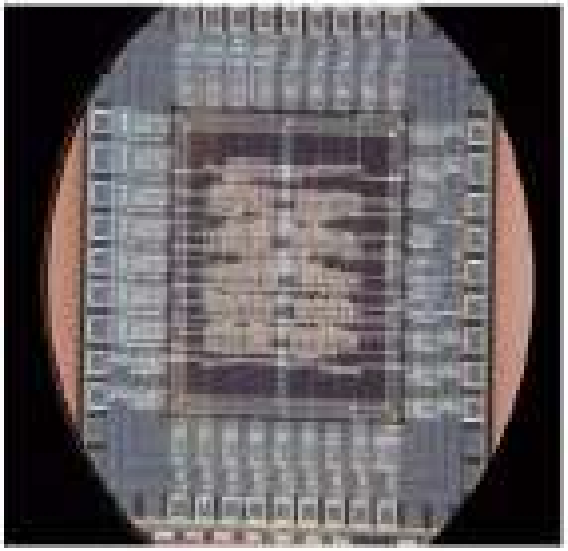
What can we do with LSI?

My Chips fully layouted with Alliance

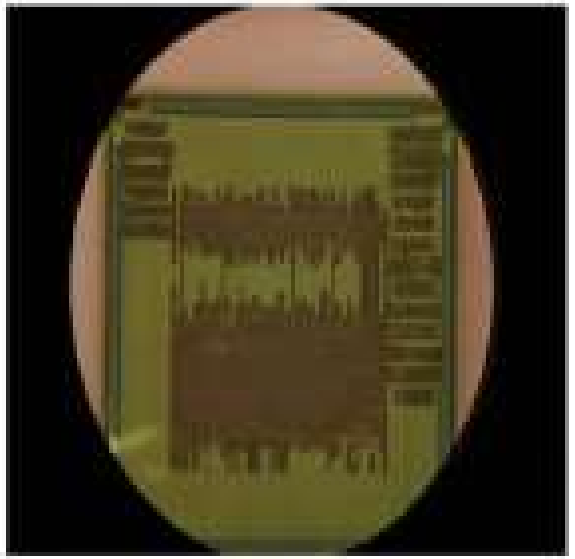
- All these chips are fabricated with VDEC shuttle.



Rohm 0.35um



Onsemi 1.2 um



Rohm 0.18um

We still need NDA for only look at the design rules!

Less expensive Fabrication effort-1

- Nano Technology Platform Japan
  - http://nanonet.mext.go.jp/english/

Nanotechnology Platform (2012-2021)
- User Facility Network Japan

- **38** groups from **26** national institutes and universities align making up one structure for ***"Share-Use Cutting-Edge Facility for Nanotechnology"***
- **Sponsorship by MEXT** for **10 years** from 2012.
- **Collaboration** among industry, government and academia.
- **Interdisciplinary research** in nanotechnology.
- Improvement in **the usability of equipment**.
- Mobilization of **human resources**.
- Collaboration between **3 technological areas** including "Nano-characterization, Analysis", "Nanofabrication", and "Molecular Synthesis and Analysis".

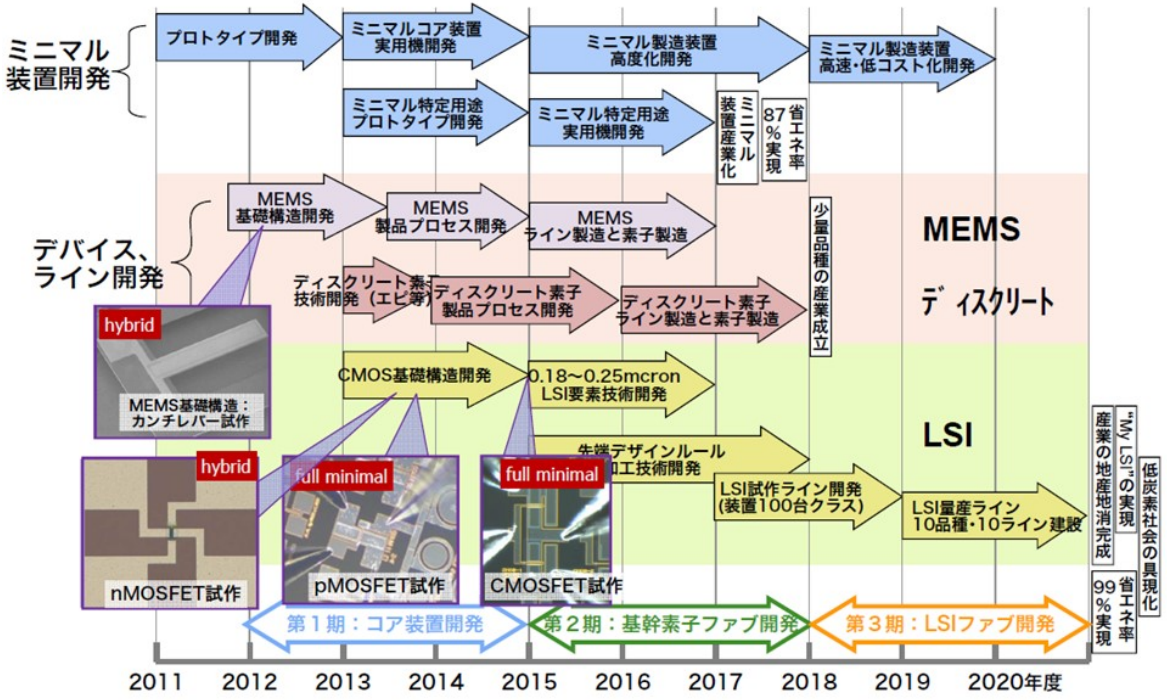
Most of the facilities only provide the equipments to share.
But **Kitakyushu Foundation for the Advancement of Industry , Science and Technology(FAIS)** provides the operational and/or materials support.

Less expensive Fabrication effort-2

- Minimal Fab

0.5” wafer, no clean room.
Low cost desktop size fabrication
Currently only MEMS
CMOS LSI will be 2020 or later

http://www.yokogawa.co.jp/semisv/minimal-fab_en.htm



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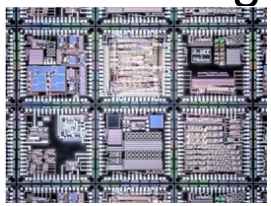
Nano Technology Platform Japan

FAIS Facility

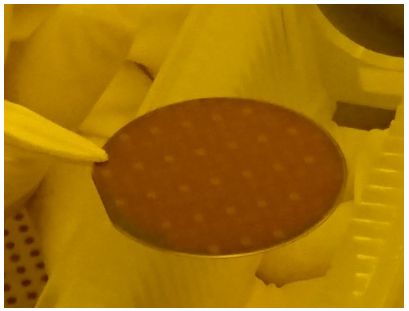
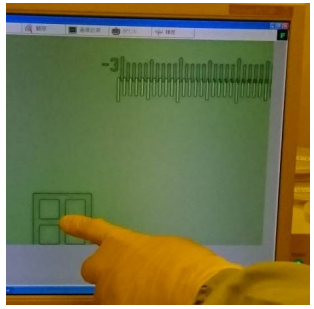
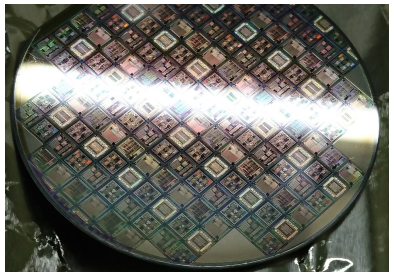
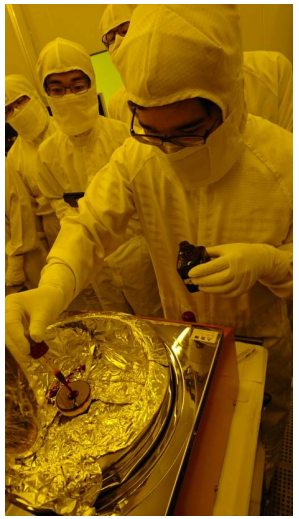
- CMOS consistent prosess support
  Applying design rules based on the Center's unique CMOS1 μm, the Center supports research and development consistently from circuit design, photomask fabrication, wafer process, assembly and testing process, and characterization to failure analysis.
- MEMS nano-technology support
  The Center supports manufacturing three-dimensional structure consisted of Si based materials mainly (microbrige, cantilever, SiN independence film, etc.) and microdisplacement sensor. Also the Center supports research and development of numerous processes for Si and various MEMS devices used crystal, quartz and sapphire substrates.
- Human resources development
  The Center conducts the education which enables human resource to create highly practical applications applied nanotechnology, along with basic education in order to use equipment safely such as safety training and operation training. The education is carried out through IC-MEMS related training seminar.

NDA Free Design rules!



FAIS 2um 2M fab. for FUN

- Fabrication cost can be as low as 400 euro.
  QFP packaged ~20 chips A shuttle service is available at 650 euro
- You can enjoy the clean room operation
- NDA free DRC and SPICE parameters.
  – Users cooperate with FAIS to capture them.
- Migration plan to Fenitech 0.6um 3M is developing without NDA.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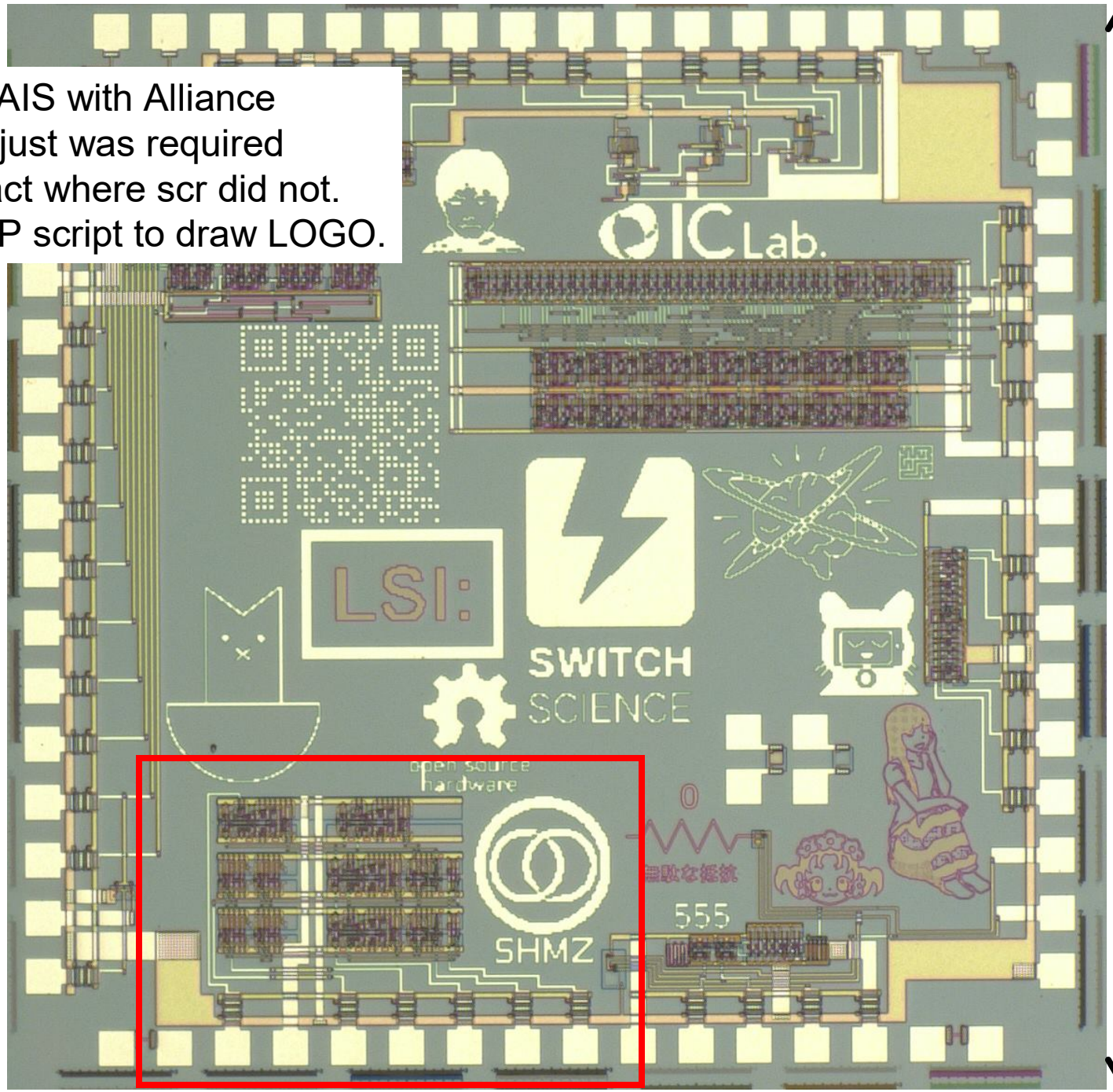
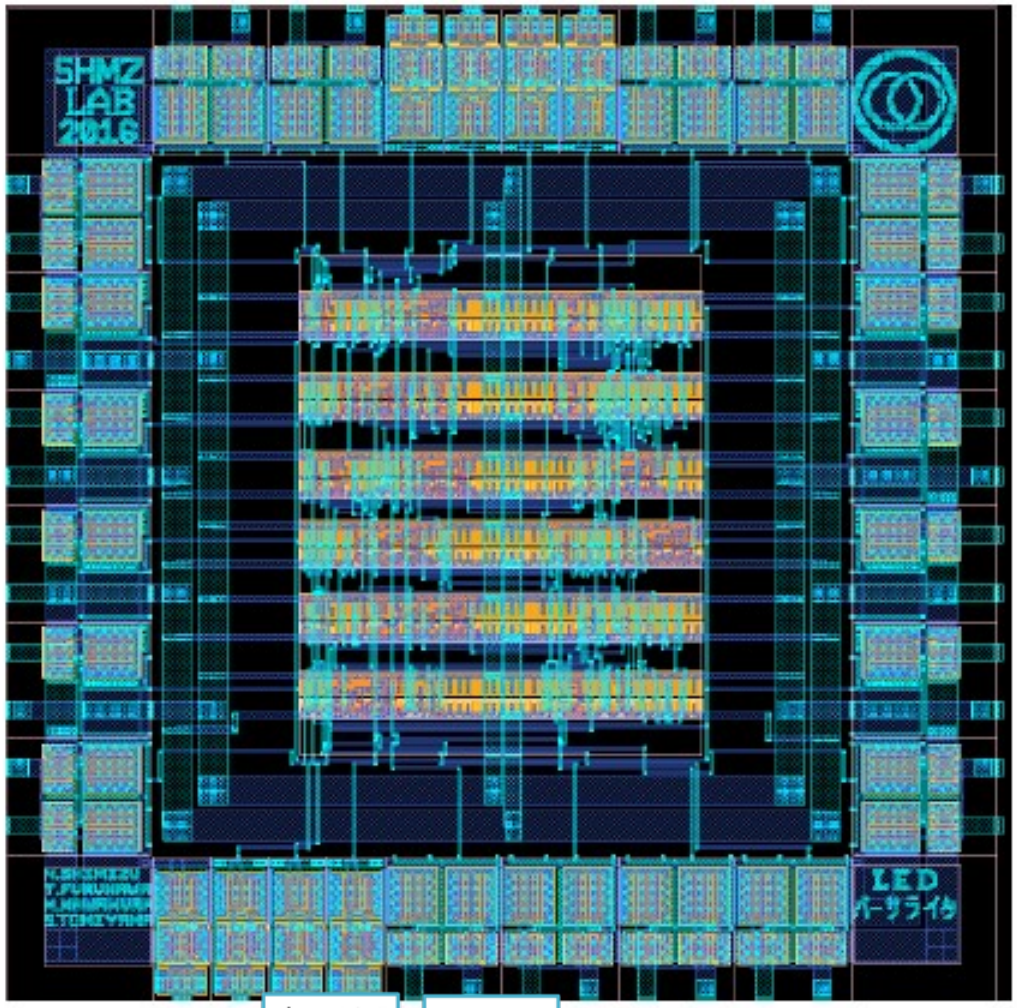
My first trial for FAIS with Alliance
Some manual adjust was required
to put body contact where scr did not.
I wrote PBM to AP script to draw LOGO.



Complete chip for FAIS only with Alliance



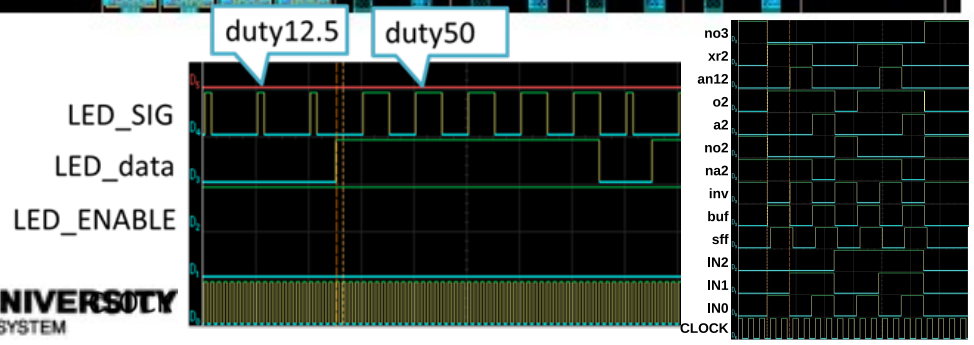
A master student, and
two undergraduates

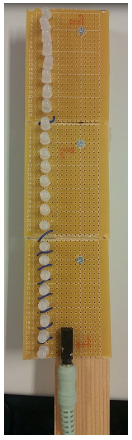
458 Tr.in core.
(Target 256, test cir. 172)
3.2mm sq. with pads.

- RESET
- CLOCK
- LED_ENABLE
- LED DATA
- Test input 4本

OUTPUT：12本

- LED_SIG





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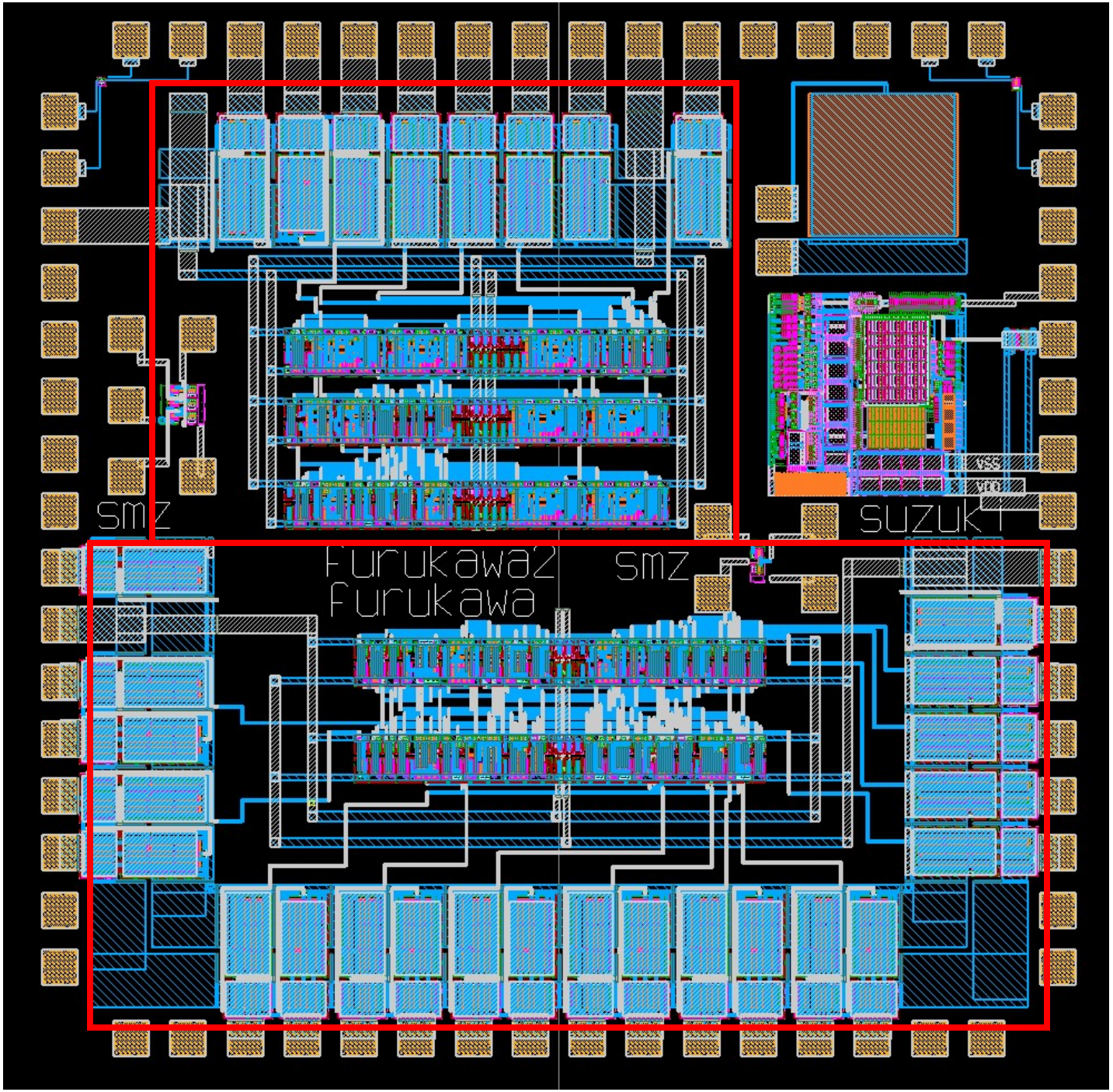
Under graduate 3rd year students project



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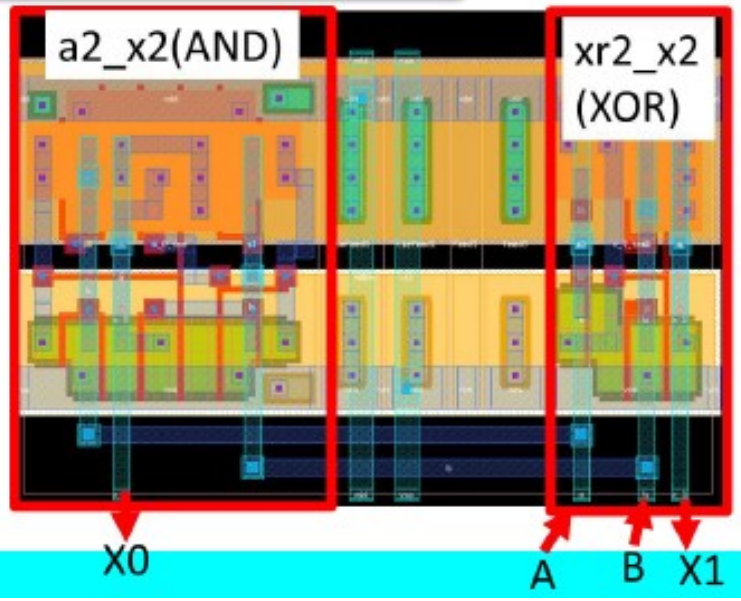
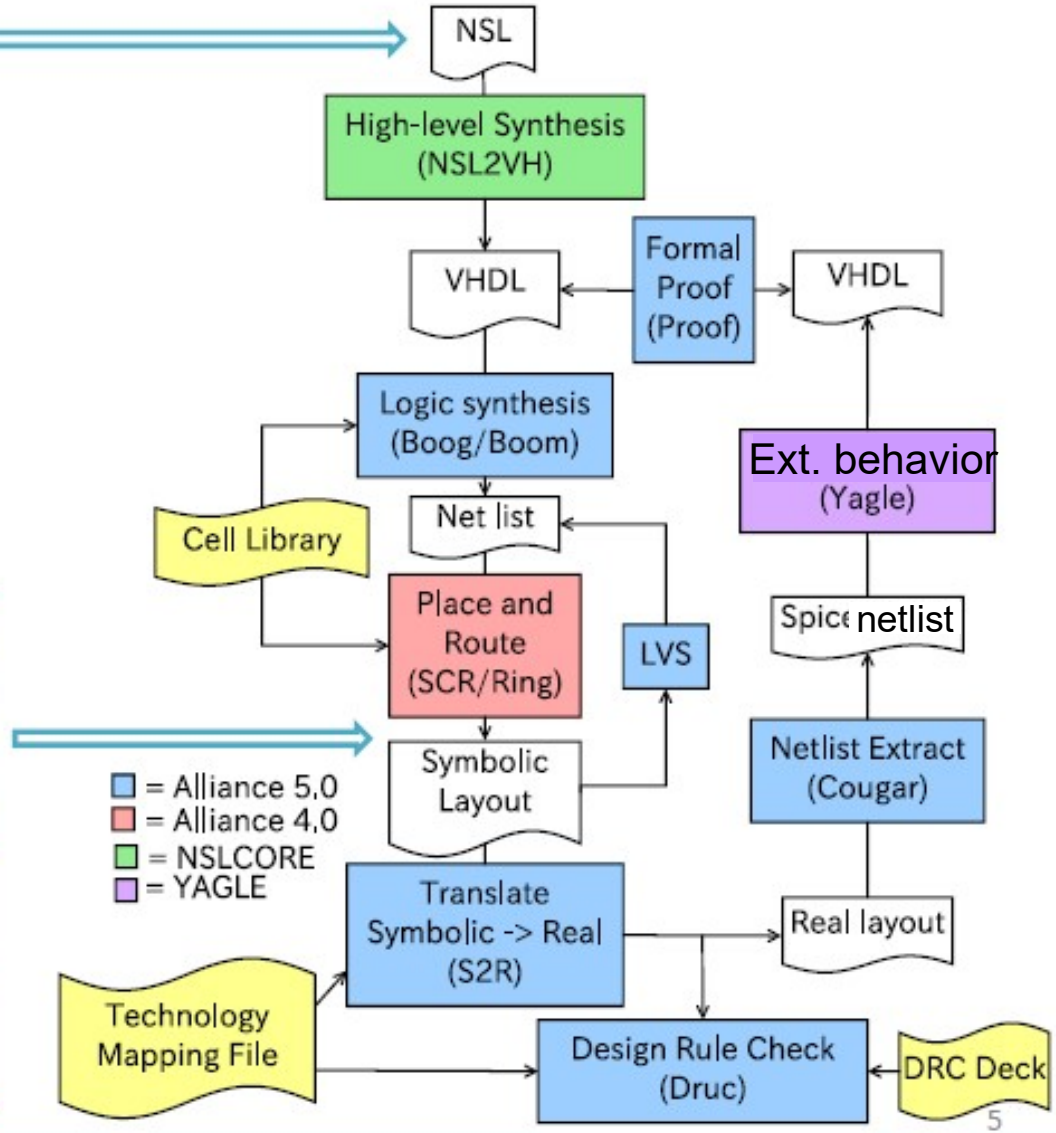
Our Design flow

NSL

```
declare adder{
  input a,b;
  output x[2];}
module adder{
  x=a+b;}
```

Symbolic layout





Our cells for Alliance/Coriolis for NDA free fabrication.

Technology	Design rules	Library in Alliance
FAIS 2um 2M	FAIS 2um	sxlib_25um
FENITECH 0.6um 3M	FAIS 2um x 0.3	sxlib_25um
TSMC 0.18um 6M*	MOSIS DEEP SUBM	nsxlib (2016)

*TSMC fab. Is not tested yet by ourselves. You can check:
https://www.mosis.com/pages/design/flows/design-flow-scmos-kits

All cells are based on sxlib and I modified to meet the DRC.
SPICE parameteres for FAIS and FENITECH is under testing.
We made test chips and got testing result. We are the way to make models.
I made nsxlib when I came LIP6 in 2016.

With the symbolic to real layout tuning ability of Alliance, we may be able to expect that these libraries work well on other technologies.

And more

- We expect more company will participate this community.
- We will support making chips by children (junior high school) with Ome sato foundation.
  http://www.sato-zaidan.or.jp/h27/kobetu-5-3-4.html
- The project Make! LSI will be explined with the slides from Prof.Akita
  https://www.facebook.com/makelsi/

Continue to Prof.Akita's slides

Is “LSI” a Tool for Everyone?

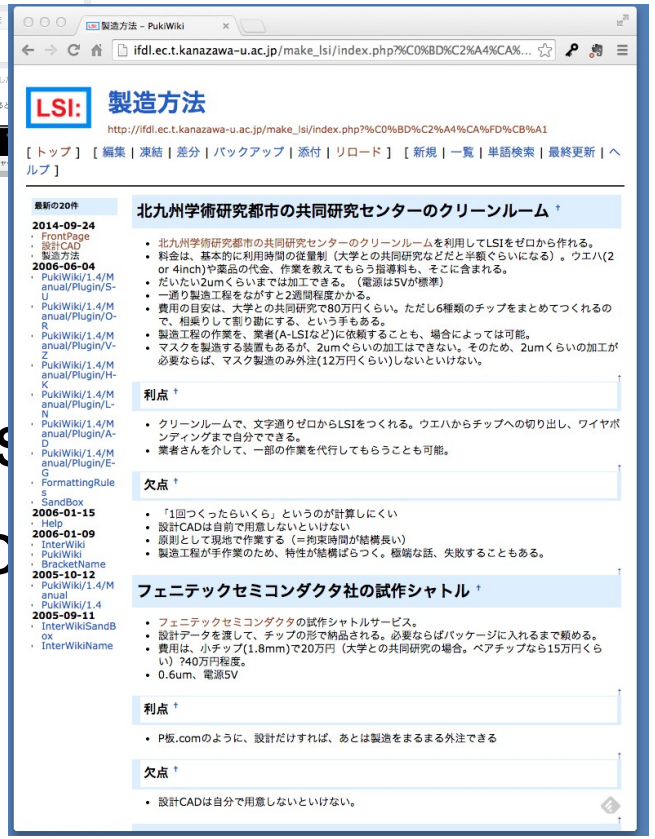
- Most people can’t imagine to “design original LSI”
  - Too expensive, Too complicated, No Experiences
- Most people simply consider to buy LSI
  - MCU, Sensors, …
  - Lots Realized
  - Restrictions in Thinking: Using Exsisting LSI
- Everyone can use Kinect, Few can invent Kinect
  - Losing Chance of Innovation

What Required for “LSI as Tool”?

- CAD Tool
  - Too Expensive Commercial Tools
  - Too Complicated CAD System
- Fabrication Service
  - Too Expensive, Too Long TAT (several months)
  - Strict NDA (prevents sharing know-hows, user community)
- User Community
  - Specialists who know not only “How to design”, but also “What to use” LSIs.

MakeLSI: - Outline

- Know-how Sharing
  - Freeware CAD
  - Basic Knowledges
- Community
  - 100+ in ML
  - LSI Specialists & Non-specialis
  - No Qualification for Contributio
- NDA-Free Fabrication
  - Lambda-rule ～1[um]



http://ifdl.jp/make_lsi

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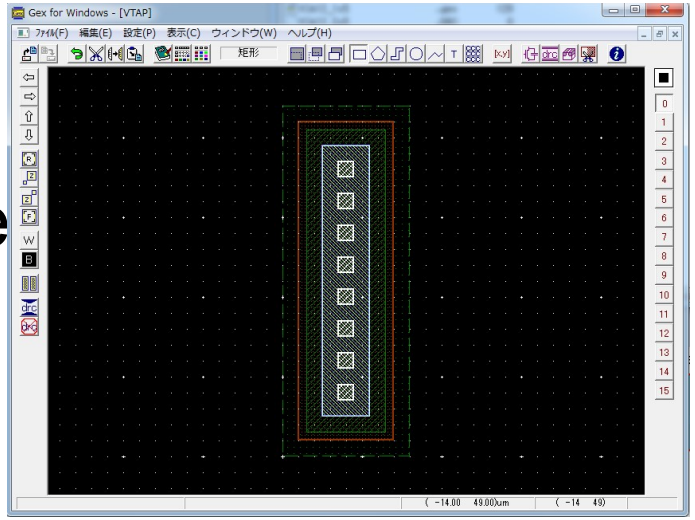
MakeLSI: - Tools

- Layout Tool: Wgex by Prof. Asada @ U.Tokyo
  - Circuit Extraction & DRC
- Circuit Simulator: LTspice / Spice3
- Logic Synthesize & P&R: Alliance

- Commonly Used in Project
  - Sharing Know-hows in usage and design
  - Integrating & Sharing IPs

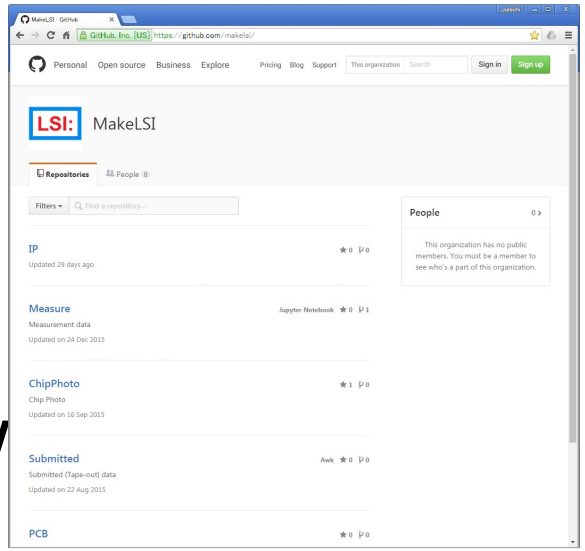


MakeLSI: - Fabrication

- Fabrication Trials with Multi Chip Project at Kitakyushu's Facilities
  - CMOS 2[um], 2Al Technology, NDA-Free
- (Preparing) Phenitec Semiconductors's Shuttle
  - CMOS 0.6[um], 3Al Technology
  - NDA-Free Design Rule based on Kitakyushu's Rule, shrinking x0.3
- (Future) minimalfab by AIST, Japan
  - 0.5in wafer, Mask-less exposure, 1week TAT

MakeLSI: - IPs

- Sharing on GitHub
  - Standard Logic Cells
  - Analog IPs (OPA, BGR)
  - MOS TEGs
- OSHW (Open Source Hardw
  - NDA-Free Design Rule
    = NDA-Free IP



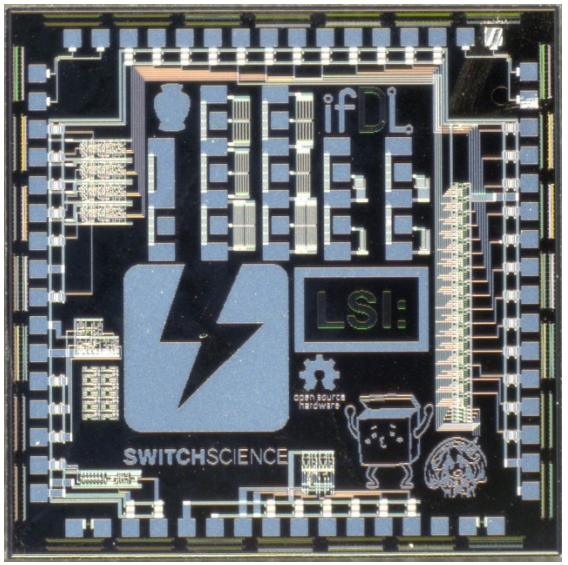
open source hardware

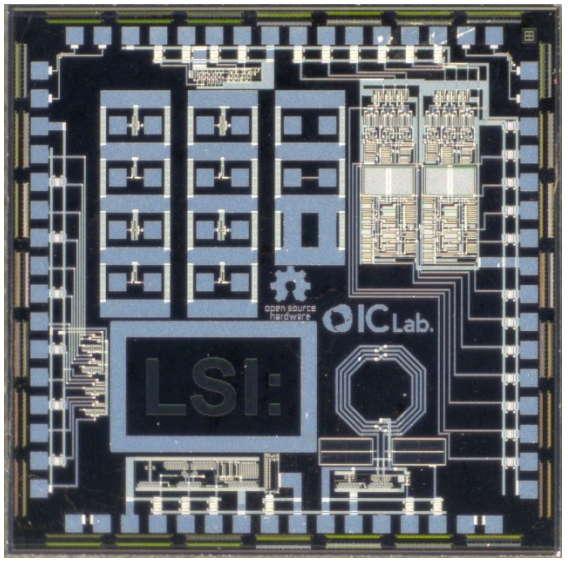
MakeLSI: - 1st Trial in 2015

- 8 Contributors
  - Free fee, Open & Share Contents
- 11 Circuits
  - Kilburn Adder
  - Guitar Effector
  - 1bit CPU
  - 4-16 Decoder
  - Ring VCO, LC-VCO, BGR

☑Saw Oscillator
☑OPA
☑MOSFET TEGs
☑Timer“555”

- Wide Variety, Passionate Activity



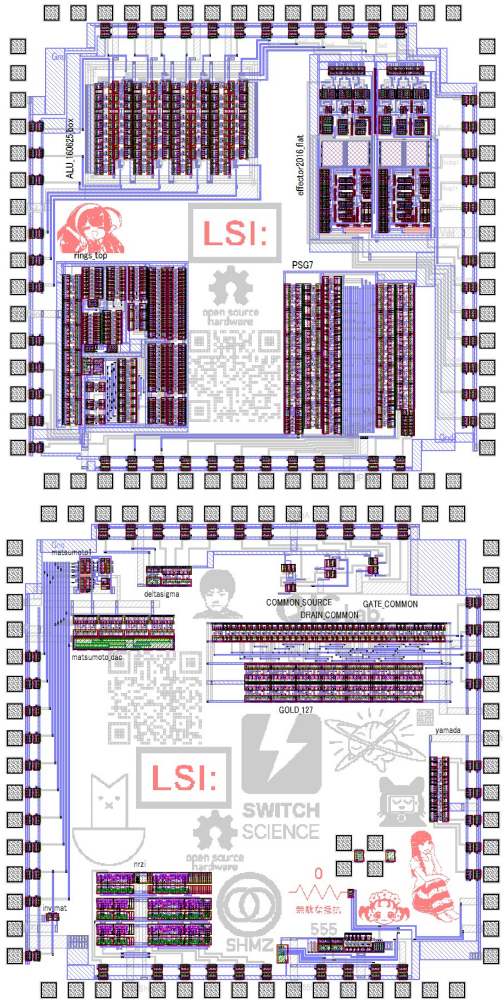


MakeLSI: - 2nd Trial in 2016

- 11 Contributors
  - Free fee, Open & Share Contents
- 12 Circuits
  - ALU
  - Guitar Effector
  - RingOSC
  - PSG
  - Delta-sigma ADC

☑R-2R DAC
☑NRZI Codec
☑GoldCoder
☑Inverter, FA
☑Timer“555”

- Wide Variety, Passionate Activity



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Distributed IP Development

- Framework=NDA-Free, Common-Technologies/Tools
- Rapid IP Development
  - Developed by lots of contributors
  - Possible Low Quality (bugs, errors, …)
  - Quality can be improved by contributors,
- Cf. OSS (Open Source Software; Linux, etc.)
  - Quality will be rapidly improved by contributors
  - Contributors' passions for development & improvement (user community)
  - Open framework (source code, license, …)required

Summary

- Effect of Moore's Law
  - High Performance & Wide Spread of Applications
- Technology MUST become a Tool for Everyone
  - Wide application, Seed of innovation
- Open Source LSI Development
  - Open framework, NDA-Free
  - Rapid development & improvement in IP