# A Smart Sensor for Automotive Vision Applications

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## Abstract

Today, robotics and intelligent vehicles need sensors with fast response time, low energy consumption, able to extract information from a real environment. There are many kinds of image acquisition system available on today's market with various applications. Despite the wide variety of these applications, all digital cameras have the same basic functional components, which consist of optical photons collection, wavelength photons discrimination (filters), timing, control and drive electronics for the sensing elements, sample/hold operators, colors processing, analogue to digital conversion and electronics interfaces.

CCDs have been the dominant technology for electronic image sensors for several decades due to their high photosensitivity, low fixed pattern noise, small pixel, and large array sizes.

However, in the last decade, CMOS image sensors have gained attention from many researchers and industries thanks to their low energy dissipation, low cost and on chip processing capability due to their integration on standard VLSI process.

To face the computational complexity induced by the computer vision algorithms, an alternative approach consists to perform some image processing on the sensor focal plane. The integration of pixel's array and image processing circuits on a single monolithic chip makes the system more compact and allows enhancing the behavior and the sensor response. To achieve low-level image processing tasks (early-vision), a silicon retina integrates analogue and/or digital processing circuits in the image-sensing element or at the edge of the image sensor array. Most often, such circuits are dedicated for specific applications. The energy dissipation is also lower than with classical approach using multi chip (microprocessor, sensor, logic glue …etc). Noise and cross-talk can also be reduced through monolithic connections instead of off-chip wires.

The paper will present a general conclusion on the aptitude of CMOS retinas to become potential candidates for systems on chip, consequently to reach an algorithm-architecture-system adequacy. In this context, an application was selected making it possible to develop a conclusion on a partial integration of a system on chip[1]. Hence the paper focuses on the VLSI compatibility of retinas, more particularly, of integrating image processing algorithms and their processors on the same sensor focal plane to provide a smart on chip vision system (System on Chip). The paper includes recommendations on system-level architecture and a design methodology for integrating image processing within a CMOS retina on a single chip. It highlights a compromise between versatility, parallelism, processing speed and resolution. Our solution aims to take also into account the algorithms response times while reducing energy consumption so as to increase the system performances for an intelligent vehicle application.

***KEYWORDS — Vision System Architecture - System on Chip – Retinas - CMOS/APS Sensors***

[1] A. Elouardi, S. Bouaziz, A. Dupret, J.O Klein, R. Reynaud, "On Chip Vision System Architecture Using a CMOS Retina". Proceeding of IEEE Intelligent Vehicle Symposium, IV'04. Pages 206-211. ISBN 0-7803-8311-7. June 14-17, 2004. Parma, Italy.